REMARKS/ARGUMENTS

Request for Continued Examination:

The applicant respectfully requests continued examination of the above-indicated application as per 37 CFR 1.114.

Claims 1-16, 20-37, 41-46, 78-83, 86-88, 90-94 and 96 are rejected under 35 USC 103(a) as being unpatentable over Bicknell et al. (US pub. 2003/0193776) in view of Meehan et al. (US pub. 2004/0177218).

Regarding 35 USC 103(a) non-obviousness, first, it is asserted by the applicant that after the amendment, the following amended independent claims have already overcome 35 USC 103(a). Second, the commercial success of secondary considerations overcoming non-obviousness should be taken into consideration by the USPTO when considering non-obviousness. A Rule 132 Declaration will follow shortly to explain the commercial success of the claimed invention.

Amended independent claims 1, 21, 78 and 90

In order to overcome the rejections in the OA of 6/23/2008 made by the examiner, the applicant adds the following limitation of claims 89 or 95, into all independent claims.

"wherein said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual IO information to transmit through the device-side IO device interconnect, and a check data segment containing check

codes derived from said payload data for checking the correctness of said payload data after transmission."

However, the reason why addition of aforesaid limitations into all independent claims has overcome the rejection is as follows:

The Examiner deemed that "said data packet comprises a start segment at the beginning indicating the start of said data packet, an end segment at the end indicating the end of the data packet, a payload data segment containing actual IO information to transmit through the device-side IO device interconnect, and a check data segment containing check codes derived from said payload data for checking the correctness of said payload data after transmission." has already been taught or suggested by paragraph 0025 of Johnson. However, applicant respectfully disagrees, argues and explains as follows:

The amended independent claims of the present invention further comprises "wherein said **data packet** comprises **a start segment** at the beginning indicating the start of said data packet, **an end segment** at the end indicating the end of the data packet, **a payload data segment** containing actual IO information to transmit through the device-side IO device interconnect, and **a check data segment** containing check codes derived from said payload data for checking the correctness of said payload data after transmission.". that is, according to the amended independent claims of the present invention, the present invention **re-formats** said device-side IO request and accompanying IO data into **at least one data packet,** in which **the data packet** comprises **the start segment** for indicating the start of said data packet to be transmitted, **the end segment** for indicating the end of the data packet to be transmitted, **the payload data segment** containing actual IO information to be

transmitted, and **check data segment** containing check codes for checking the correctness of said payload data after transmission (as to detailed descriptions of the data packet, please refer to Fig.10 and para.0071 and 0072 of the present invention).

In contrast, paragraph 0025 of Johnson only discloses "several parameters, such as **Initial Strip Size for indicating the size (i.e., the number of bytes) of the initial block of data** (e.g., metadata or header information) to be transferred for the first stripe of the drive, **an Initial Skip Size for indicating an amount of the drive** (i.e., the number of bytes) to skip prior to transferring data for the drive, **a Stripe Size for indicating the size** (i.e., the number of bytes) in a single stripe, and **a Stripe Skip for indicating the amount of the drive to skip** after transferring a stripe of data. Alternatively, parameter information may included **a set of absolute addresses,** each having **a start address and an end address, that determine the data that is to be transferred from host memory to the disk drives or determine where data is to be stored when transferred from the disk drives to host memory".** From the aforesaid paragraphs, it can be concluded that para.0025 of Johnson only disclose as follows:

(a1) **Initial Strip Size** for indicating the size (i.e., the number of bytes) of the initial block of data;

(a2) **an Initial Skip Size** for indicating an amount of the drive (i.e., the number of bytes) to skip prior to transferring data for the drive;

(a3) **a Stripe Size** for indicating the size (i.e., the number of bytes) in a single strip;

(a4) **a Stripe Skip** for indicating the amount of the drive to skip; and

(a5) **a set of absolute addresses,** each having **a start address and an end address**, which of which determine the data that is to be transferred from host memory to the disk drives or determine where data is to be stored when transferred from the disk drives to host memory.

Please be noted that, in the claimed invention, "**the start segment**" is a segment in a data packet indicating the beginning of the data packet, which tells the receiving device that a new data packet is now being transmitted to and will be received by the receiving device, while "**a start address**" disclosed in the Johnson tells the receiving device where in the memory, it can access the data, and if the receiving device of such information has the function of performing data access, it can access the data in the memory according to the start address. Therefore, "**the start segment**" in the claimed invention and "**a start address**" disclosed in the Johnson are totally different from each other. Similarly, in the claimed invention, "**the end segment**" is a segment in a data packet for indicating the end of the data packet, which tells the receiving device that the data packet has being transmitted to completion and will be no more data belonging to that data packet being transmitted to the receiving device, while "**an end address**" disclosed in the Johnson tells the receiving device where in the memory the last data to be transferred exists, and if the receiving device of such information has the function of performing data accessing, it can access the last data in the memory according to the end address. Therefore, "**the end segment**" in the claimed invention and "**an end address**" disclosed in the Johnson are totally different from each other.

In conclusion, para. 0025 of Johnson disclosed something totally different from amended independent claims of the claimed invention. Therefore, para.0025 of

Johnson **fails to teach or suggest such a data packet** for transmission to said PSD, in which **the data packet** comprises **the start segment** for indicating the start of said data packet to be transmitted, **the end segment** for indicating the end of the data packet to be transmitted, **the payload data segment** containing actual IO information to be transmitted, and **check data segment** containing check codes for checking the correctness of said payload data after transmission" in claims 89 and 95 of the present invention.

The following will explain some of the features of the claimed invention, which, the applicant believes, have never been taught or discloses by all cited references.

Point 13 in the OA

Claims 13 and 29 of the present invention claim **wherein said storage virtualization controller is configured to present redundantly a logical media unit on at least two of said plurality of host-side device interconnect ports.**

Moreover, please refer to paragraph [0098] of the present invention, in which another feature that an SVC might typically implement is redundancy in the host-side interconnects in which multiple host-side interconnect ports are included on the SVC and **LMUs are presented to the host identically over two or more of these interconnects.** This feature is designed to allow the host the ability to maintain access to the LMU even if one of the interconnects and/or ports on the interconnect should break, become blocked or otherwise malfunction. That is, said storage virtualization controller is **configured to present redundantly a logical media unit on at least two**

of said plurality of host-side device interconnect ports twice.

In contrast, paragraph 0019 of Bicknell only discloses "Disc drive 106 also includes a data interface 144.....due to disc drive failure", Please refer to Fig. 6 of Bicknell, in which two controllers, CONTROLLER 1 and CONTROLLER 2, are shown and each has only one interconnect coupled to a HOST COMPUTER to its left. Obviously, Bicknell does not disclose or suggest a controller having two ports connecting to a host for redundantly presenting a LMU to the host. Therefore, Bicknell fails to teach or suggest **"wherein said storage virtualization controller is configured to present redundantly a logical media unit on at least two of said plurality of host-side device interconnect ports."**

Point 22 in the OA

Amended Claims 34 and new claims 101, 102 and 103 of the present invention claim **"wherein said group of PSDs include a first set of PSDs and a second set of PSDs, said first set of PSDs and said second set of PSDs are not received in a same enclosure, and said storage virtualization controller further comprises at least one multiple-device device-side expansion port for coupling to said second set of said PSDs."**

Please refer to paragraph [0092] of the present invention. Because the S-ATA specification only allows for maximum signal line lengths of 1.5 meter, the PSDs connected to one SVC must be packed close enough so that no signal line length exceeds 1.5meter. A typical S-ATA storage virtualization subsystem will only provide for connection of a maximum of 16 S-ATA PSDs because of these limitations. So, a

"pure" S-ATA storage virtualization subsystem is unable to match the expandability of a Fibre FC-AL storage virtualization subsystem, which will typically allow for connection of up to 250 PSDs via connection of external expansion chassis on the same set of device-side IO device interconnects. [0093] In order to overcome this limitation, the present invention optionally includes one or more expansion device-side multiple-device IO device interconnects, herein referred to as device-side expansion ports, such as Parallel SCSI or Fibre FC-AL on the SVC. These interconnects will typically be wired in such a way as to allow external connection of external expansion chassis. These chassis could be simple "native" just a bunch of drives (JBODs) of PSDs directly connected to the interconnect without any intervening conversion circuitry or could be intelligent JBOD emulation subsystems that emulate "native" JBODs using a combination of S-ATA or P-ATA PSDs and a single or redundant set of SVCs that provide the conversion from the multiple-device IO device interconnect protocol that provides the connection of the JBOD subsystem to the primary storage virtualization subsystem to the device-side IO device interconnect (S-ATA or P-ATA) protocol that provides the connection between the JBOD SVC(s) and the PSDs that they manage. Therefore, in the claims of the present invention, said storage virtualization controller further comprises at least one multiple-device device-side expansion port for coupling to said second set of said PSDs.

Moreover, please refer to figs. 3, 17 and 18, in which in fig.3, there are 16 S-ATA interconnects 201 connected to **local** physical storage device array (PSD) 400 which comprises a plurality of physical storage devices 420 **(i.e., said first set of**

PSDs in claims 34 and new claims 101, 102 and 103). However, please refer to figs. 17 and 18, in which in addition to the 16 Serial ATA interconnects that are connected to local PSD 400 (please refer to fig.3), storage virtualization controller (SVC) can optionally have more **expansion subsystems (i.e., said second set of said PSDs in claims 34 and new claims 101, 102 and 103) through the device-side expansion port for coupling to said second set of said PSDs (i.e., said expansion subsystem which is indicated by dotted lines in figs. 17 and 18).**

In contrast, the Midplane Card ports 209 of Fig. 6 of Bicknell only discloses the midplane card ports 209 are connected to data ports 204 of controller, which does not disclose a second set of HDDs, and thus fails to teach or suggest "**wherein said group of PSDs include a first set of PSDs and a second set of PSDs, said first set of PSDs and said second set of PSDs are not received in a same enclosure, and said storage virtualization controller further comprises at least one multiple-device device-side expansion port for coupling to said second set of said PSDs."** In claims 34 and 96 of the present invention

Point 37 in the OA

Regarding new claims 97, 98 and 99

New claims 97, 98 and 99 of the claimed invention claim "wherein said group of PSDs are received in a plurality of enclosures." Please refer to Figs 17 and 18 and paragraph [0093], in which [0093] In order to overcome this limitation, the present invention optionally includes one or more expansion device-side multiple-device IO device interconnects, herein referred to as device-side expansion ports, such as

Parallel SCSI or Fibre FC-AL on the SVC. These interconnects will typically be wired in such a way as to allow external connection of external expansion chassis. These chassis could be simple "native" just a bunch of drives (JBODs) of PSDs directly connected to the interconnect without any intervening conversion circuitry or could be intelligent JBOD emulation subsystems that emulate "native" JBODs using a combination of S-ATA or P-ATA PSDs and a single or redundant set of SVCs that provide the conversion from the multiple-device IO device interconnect protocol that provides the connection of the JBOD subsystem to the primary storage virtualization subsystem to the device-side IO device interconnect (S-ATA or P-ATA) protocol that provides the connection between the JBOD SVC(s) and the PSDs that they manage. That is, the expansion subsystem(indicated by dotted lines) in figs. 17 and 18 and PSDs (not shown but coupled to the SVC through Serial-ATA interconnected as shown in fig. 17 and 18) of storage virtualization subsystem (indicated by dotted lines) **are received in a plurality of enclosures(different enclosures).**

In contrast, the applicant asserts that all cited reference fails to teach or suggest "wherein said group of PSDs are received in a plurality of enclosures."

Thus, all pending claims are submitted to be in condition for allowance with respect to the cited art for at least the reasons presented above. The Examiner is encouraged to telephone the undersigned if there are informalities that can be resolved in a phone conversation, or if the Examiner has any ideas or suggestions for further advancing the prosecution of this case.

Sincerely yours,

/Winston Hsu/ Date: 12/19/2008

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 13 hours behind the Taiwan time, i.e. 9 AM in D.C. = 10 PM in Taiwan.)